MULTIMEDIA UNIVERSITY

STUDENT ID NO

MULTIMEDIA UNIVERSITY

FINAL EXAMINATION

TRIMESTER 2 2022/2023 (TERM ID 2220)

EEE4186 – VLSI SYSTEM DESIGN AND MODELING TECHNIQUE

8 JULY 2023

9:00 AM – 11:00 AM
(2 Hours)

INSTRUCTION TO STUDENTS

1. This Question paper consists of **4 pages** including cover page with **4 Questions** only.

2. Attempt **ALL FOUR** questions. All questions carry equal marks and the distribution of the marks for each question is the same.

3. Please print all your answers in the answer Booklet provided.

Question 1:

(a) Based on Figure Q1a, compute the characteristic equations of the output signals, S and Cout for the system, FA.

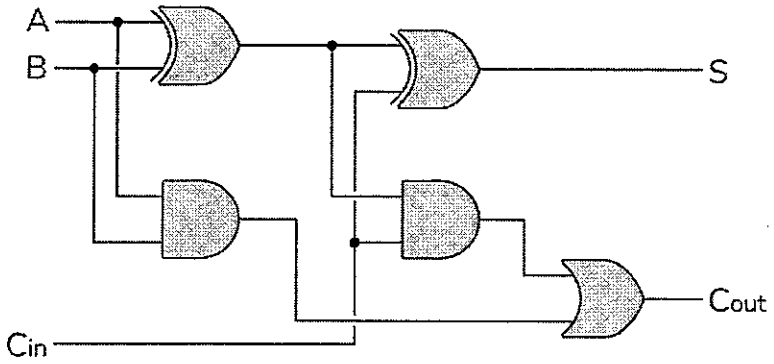

Figure Q1a

[4 marks]

(b) Design the circuit shown in Figure Q1a using Verilog codes in the following modeling methods:

(i) Gate-level modeling method

(ii) Logical operators modeling method

[7 + 6 marks]

(c) From Part (b), design the system FA2 using Verilog codes for Figure Q1b. You may use the structural model, vectored signals and system, FA created in Part (b).

[8 marks]

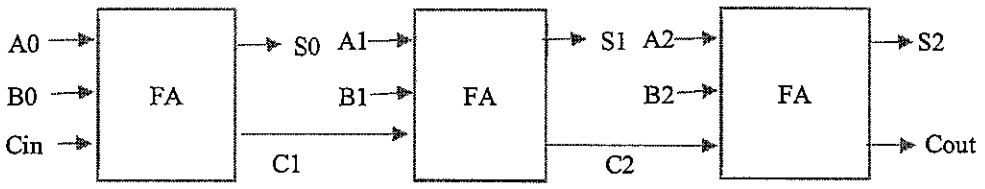

Figure Q1b

Question 2:

(a) Design a 16-to-1 multiplexer (mux16) using the If-else Verilog statement.

[12 marks]

(b) Design a 16-to-1 multiplexer (mux16) using the Case Verilog statement.

[13 marks]

Continued ...

Question 3:

(a) Design a finite state machine based on the states shown in Table Q3 using Verilog code.

[13 marks]

Table Q3: FSM1

Current State	Next State		Output, Z	
	Input, X = 0	Input, X = 1	Input, X = 0	Input, X = 1
A	A	B	0	0
B	C	A	0	1
C	D	C	1	1
D	B	D	1	0

(b) Design a finite state machine as shown in Figure Q3 using Verilog code. The finite state machine shown in Figure Q3 consists of input signals; X, rst, clk and an output signal, Z.

[12 marks]

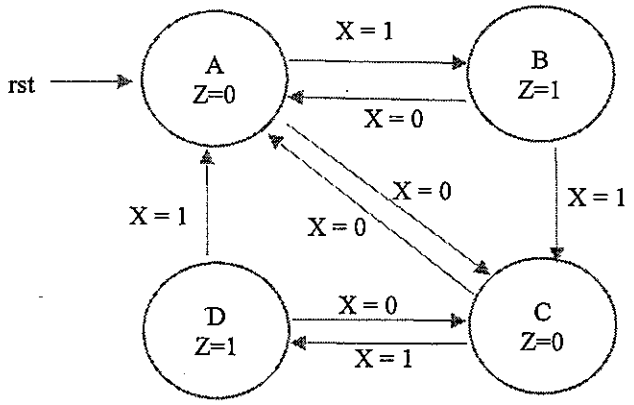

Figure Q3: FSM2

Continued ...

Question 4:

(a) Design a 4-bit Arithmetic Unit based on the functions shown in Table Q4a. [13 marks]

Table Q4a: Arith_unit

Operation code (opcode)	Function, Z
000	A + 0 + 0
001	A + B
010	A + B + 1
011	A – B
100	A + 1
101	A – 1
110	B + 1
111	B – 1

(b) Design a 4-bit Logic Unit based on the functions shown in Table Q4b. [12 marks]

Table Q4b: Logic_unit

Operation code (opcode)	Function, Z
000	A or B
001	A and B
010	A xor B
011	A xnor B
100	A nand B
101	A nor B
110	Not A
111	Not B

End of Paper